What is claimed is:

1. A method of aligning clock signals in a bus system comprising a master and one or more slave devices connected via a channel, the bus system further comprising a first system clock propagating towards the master and a second system clock propagating away from the master, and the master further comprising a transmitter and a receiver, the method comprising:

generating a transmit clock signal in the master, wherein data is driven onto the channel in relation to the transmit clock signal;

arbitrarily adjusting the phase of the transmit clock signal while maintaining a fixed phase relationship between the transmit clock signal and the second system clock.

2. The method of claim 1, wherein the master transmitter introduces a transmit output delay into data signals driven onto the channel, and wherein the fixed phase relation between the transmit clock signal and the second system clock equals 90° plus the transmit output delay.

3. The method of claim 2, the method further comprising:

providing a receive clock signal in the master, where data is read from the channel by the master in relation to the receive clock signal; and

further adjusting the phase of the transmit clock signal to have a fixed phase relationship with the receive clock signal while maintaining the fixed phase relationship between the transmit clock signal and the second system clock.

4. The method of claim 3 wherein the fixed phase relationship between the transmit clock signal and the receive clock signal is 180°.

5. A method of aligning clock signals in a bus system comprising a master and one or more slave devices connected via a channel, the bus system further comprising a first system clock propagating towards the master and a second system clock propagating away from the master, wherein the first and second system clocks are initially phase aligned, the method comprising:

generating a transmit clock signal in the master in relation to the first system clock;

shifting the transmit clock signal phase by 90°; and

passing the phase shifted transmit clock signal through an output driver circuit in the master to generate the second system clock, whereby the first and second system clocks are no longer phase aligned.

6. The method of claim 5, further comprising:

driving data onto the channel in accordance with the transmit clock signal; and

wherein the step of passing the phase shifted transmit clock signal through an output driver circuit drives the second system clock onto the channel, such that the data and the second system clock are communicated to the one or more slave devices via the channel in a fixed phase relationship.

7. The method of claim 6, wherein the step of generating the transmit clock signal in the master further comprises:

receiving the first system clock as a first input to a delay locked loop circuit;

receiving a phase feedback signal as a second input to the delay locked loop circuit; and

providing the output of the delay locked loop circuit as the transmit clock signal.

8. The method of claim 7, wherein the phase feedback signal is generated by phase comparing the complement of the transmit clock signal and a receive signal in a phase detector circuit.

9. The method of claim 7, wherein the phase feedback signal is generated by the output of a flip-flop circuit receiving the first system clock as an input and being gated by the complement of the transmit system clock.

10. A method of aligning system clocks in a bus system comprising a master and one or more slave devices connected via a channel, the master further comprising a receiver having a receiver setup time delay and an output driver having an output driver delay, the method comprising:

generating a first system clock external to the master such that the first system clock propagates via the channel through the one or more slave towards the master;

in the master, generating a second system clock having a phase relation to the first system clock defined such that, the phase difference between the first system clock and the second system clock is substantially equal to 90° minus the sum of the receiver setup delay and the output driver delay.

11. The method of claim 10, further comprising:

modifying the second system clock to preserve the phase relation in response to a change in the output driver delay.

12. A method of providing an apparent delay for data traversing a bus system, the bus system comprising a channel connecting a master and a plurality of slave devices, wherein data traverses the channel from the slave devices to the master in relation to a first system clock and wherein data traverses the channel from the master to the plurality of slave devices in relation to a second system clock, the method comprising:

for each slave device, calculating a fractional delay and a cycle delay, such that the sum of the fractional delay and the cycle delay with an intrinsic delay and a clock phase delay equals the apparent delay;

modifying the second system clock in the master;

for each slave device, recalculating the fractional delay in accordance with the modified second system clock.

13. The method of claim 12, wherein the master further comprises a transmitter providing an output driver delay to data and control information signals sent from the master to the slave devices, wherein the second system clock is modified in accordance a change in the output driver delay, and wherein the step of recalculating the fractional delay tracks out the change in the output driver delay.

14. The method of claim 12, further comprising:

for each slave device, following the recalculation of the fractional delay, recalculating the cycle delay.

15. The method of claim 14, wherein recalculating the cycle delay comprises:

determining whether recalculation of the fractional delay has resulted in the crossing of a cycle delay boundary.

16. A circuit for defining a second system clock in a bus system comprising a master connected to one or more slave devices via a channel, the channel communicating an externally generated first system clock towards the master, the circuit comprising:

a delay locked loop circuit receiving the first system clock and a phase feedback signal as inputs and generating a transmit clock signal;

a 90° block receiving the transmit system clock and generating a 90° phased shifted version of the transmit clock signal; and

an output driver circuit receiving the 90° phased shifted version of the transmit clock signal and generating the second system clock.

17. The circuit of claim 16 further comprising:

a zero degree phase detector receiving a receive clock signal and a complement of the transmit clock signal as inputs and generating the phase feedback signal.

18. The circuit of claim 16 further comprising:

a flip-flop circuit receiving the first system clock as an input and receiving a complement of the transmit clock signal as a gating signal and generating the phase feedback signal.

19. The circuit of claim 16, further comprising a plurality of data output drivers connected to the channel and enabled by the transmit clock signal.

20. The circuit of claim 16, further comprising a plurality of data output drivers connected to the channel and enabled by a complement to the receive clock signal.

21. A method of aligning clock signals in a bus system comprising a master and one or more slave devices connected via a channel, the bus system further comprising a first system clock propagating towards the master and a second system clock propagating away from the master, the method comprising:

initially generating a transmit clock signal in the master;

initially generating a receive clock signal in the master, wherein the receive clock is substantially complementary to the transmit clock;

initially calibrating a delay in relation to a phase relationship between the receive clock and the transmit clock;

defining the second system clock in relation to the first system clock and a delay.

22. A circuit defining a second system clock in a bus system comprising a master connected to one or more slave devices via a channel, the channel communicating an externally generated first system clock towards the master, the circuit comprising:

a delay locked loop circuit receiving the first system clock and a second phase feedback signal as inputs and generating a transmit clock signal;

a 90° block receiving the transmit system clock and generating a 90° phased shifted version of the transmit clock signal;

an output driver circuit receiving the 90° phased shifted version of the transmit clock signal and generating the second system clock;

a first phase detector receiving a receive system clock and the transmit system clock and generating first phase feedback signal;

a delay element receiving the first system clock and the first phase feedback signal and generating delayed first system clock;

a second phase detector receiving the delayed first system clock and the second system clock and generating the second phase feedback signal.